LISTING OF CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor device of a polysilicon gate electrode structure having three or more different Fermi levels, wherein:

a P type polysilicon having a lowest Fermi level is disposed on a first N type surface channel MOS transistor,

a first N type polysilicon having a highest Fermi level is disposed on a second N type surface channel MOS transistor, and

a second N type polysilicon having an intermediate Fermi level between the highest and the lowest Fermi levels and doped with both an N type impurity and a P type impurity is disposed on a P channel MOS transistor.

2. (Original) A semiconductor device according to claim 1, wherein: the P channel MOS transistor and the second N type surface channel MOS transistor are disposed in a peripheral circuit while the first N type surface channel MOS transistor is disposed in a memory cell.

3. (Original) A semiconductor device according to claim 1, wherein: the second N type polysilicon containing both the P type impurity and the N type impurity has impurity concentration distribution in which the concentration of at least the N type impurity at an upper surface of the second N type polysilicon is higher than an average concentration in the second N type polysilicon.

4. (Original) A method of producing a semiconductor device according to claim 1, wherein: the second N type polysilicon containing both the P type impurity and the N type impurity is formed by doping at least the N type impurity by use of ion implantation.

5. (Original) A method of producing a semiconductor device according to claim 1, wherein: the P type polysilicon, the first N type polysilicon, and the second N type polysilicon are separately formed by use of two masks.

6. (Original) A method of producing a semiconductor device according to claim 1, wherein: the second N type polysilicon doped with both the N type impurity and the P type impurity is formed by simultaneously activating phosphorus and boron.

7. (Original) A method according to claim 6, wherein: diffusion of boron towards a substrate is suppressed by simultaneously activating phosphorus and boron.

8. (Currently Amended) A semiconductor device including a DRAM having a gate electrode of a polymetal structure, according to claim 1 ~~comprising: an N^+ gate PMOS containing both a P type impurity ana an N type impurity and an N^+ gate NMOS which are disposed in a peripheral circuit, and a P^+ gate surface channel NMOS containing a P type impurity alone which is disposed in a memory cell~~.

9. (Previously Presented) A semiconductor device according to claim 1, wherein said P type polysilicon having the lowest Fermi level and disposed on the first N type surface channel MOS transistor is formed on a p-well for its substrate.

10. (Previously Presented) A semiconductor device according to claim 1, wherein the concentration of the p type impurity that is injected into the first N type surface channel is reduced such that a pn junction leak current is reduced.

11. (Previously Presented) A semiconductor device according to claim 1, wherein the P type polysilicon having the lowest Fermi level and disposed on the first N type surface channel MOS transistor has a lower boron content than the first N type polysilicon having the highest Fermi level and disposed on the second N type surface channel MOS transistor.

12. (Previously Presented) A semiconductor device of a polysilicon gate electrode structure having three or more different Fermi levels, the semiconductor device comprising:

a P type polysilicon having a lowest Fermi level, the P type polysilicon being disposed on a first N type surface channel MOS transistor,

a first N type polysilicon having a highest Fermi level, the first N type polysilicon being disposed on a second N type surface channel MOS transistor, and

a second N type polysilicon having an intermediate Fermi level between the highest and the lowest Fermi levels and doped with both an N type impurity and a P type impurity, the second N type polysilicon being disposed on a P channel MOS transistor, and being formed by simultaneously activating both the N-type and P-type dopants.

13. (Previously Presented) A semiconductor device according to claim 12, wherein the N-type and P-type dopants are phosphorus and boron and wherein diffusion of boron towards a substrate is suppressed by simultaneously activating the phosphorus and boron dopants.

14. (Previously Presented) A semiconductor device according to claim 12, wherein the P channel MOS transistor and the second N type surface channel MOS transistor are disposed in a peripheral circuit while the first N type surface channel MOS transistor is disposed in a memory cell.

15. (Previously Presented) A semiconductor device according to claim 12, wherein the second N type polysilicon containing both the P type impurity and the N type impurity has impurity concentration distribution in which the concentration of at least the N type impurity at an upper surface of the second N type polysilicon is higher than an average concentration in the second N type polysilicon.

16. (Previously Presented) A semiconductor device according to claim 12, wherein the second N type polysilicon containing both the P type impurity and the N type impurity is formed by doping at least the N type impurity by use of ion implantation.

17. (Previously Presented) A semiconductor device according to claim 12, wherein the P type polysilicon, the first N type polysilicon, and the second N type polysilicon are separately formed by use of two masks.

18. (Previously Presented) A semiconductor device according to claim 12, wherein said P type polysilicon having the lowest Fermi level and disposed on the first N type surface channel MOS transistor is formed on a p-well for its substrate.

19. (Previously Presented) A semiconductor device according to claim 12, wherein the concentration of the p type impurity that is injected into the first N type surface channel is reduced such that a pn junction leak current is reduced.

20. (Previously Presented) A semiconductor device according to claim 12, wherein the P type polysilicon having the lowest Fermi level and disposed on the first N type surface channel MOS transistor has a lower boron content than the first N type polysilicon having the highest Fermi level and disposed on the second N type surface channel MOS transistor.